

ABSTRACT

An microcomputer is provided including a processor and a debug circuit including a dedicated link which transfers information between the processor and debug circuit to support debugging operations. In one aspect, the processor provides program counter information, which is stored in a memory-mapped register of the debug circuit. The program counter information may be a value of the processor program counter at a writeback stage of a processor pipeline. Also, trace information including message information is transferred in a non-intrusive manner over the dedicated link. In one aspect, the microcomputer is implemented as a single integrated circuit.

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